REMARKS

Claim Rejections

Claims 25-28, 33-34, 36, and 39 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. (U.S. 6,765,152) in view of Jiang et al. (U.S. Pub. 2003/0164556). Claims 29-30 and 35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. and Jiang et al. in view of Klein et al. (U.S. 2004/0145051). Claim 31 is rejected under 35 U.S.C. §103(a) as being unpatentable over Giri et al. and Jiang et al. in view of Kikuma et al. (U.S. 6,621,169). Claim 32 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. and Jiang et al. in view of Koopmans (U.S. 2004/0035840). Claim 38 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. and Jiang et al. in view of Higgins III (U.S. 5,583,377).

Claim Amendments

By this Amendment, Applicant has amended claim 25 of this application to better protect what Applicant regards as the invention. It is believed that the amended claims specifically set forth each element of Applicant's invention in full compliance with 35 U.S.C. § 112, and define subject matter that is patentably distinguishable over the cited prior art, taken individually or in combination.

As a preliminary matter, Applicant notes that in the outstanding Office Action the Examiner has replaced Fjelstad et al. with Jiang et al., but otherwise maintained the prior rejections. As a result, in order to not further burden the record, Applicant chooses to maintain the prior arguments regarding the remaining art and will focus below on the newly cited reference to Jiang et al.

The amended claims are directed toward: a flip-chip package comprising: a) a substrate having: i) a top substrate surface; ii) a bottom substrate surface; and iii) a substrate opening extending through the top surface and the bottom surface; b) a dummy die being a silicon substrate having no electrically calculating function, connected to the bottom substrate surface and aligned with the substrate opening, and having a redistribution layer, the redistribution layer having a plurality of flip-chip pads and a plurality of connecting pads connected by an integrated circuit trace, the

plurality of flip-chip pads and the plurality of connecting pads are located on a top surface of the dummy die below the substrate opening, the plurality of connecting pads of the redistribution layer are electrically connected to the substrate, wherein the dummy die has an exposed surface located on a bottom thereof, the exposed surface having a metal thermal-conducting layer directly formed thereon to substantially cover the exposed surface located on the bottom of the dummy die, ***the metal thermal conducting layer being a non-patterned layer***, the metal thermal conducting layer ***being electrically isolated from the redistribution layer***; and c) a chip located in the opening and having a plurality of bumps electrically connected to the plurality of flip-chip pads of the redistribution layer.

In the present invention, a dummy die 230, having no electrically calculating function, includes a bottom surface having a high thermal-conducting metal layer 233 configured to dissipate heat from the chip package. Since the high thermal-conducting metal layer 233 is configured to conduct heat and not electricity, the metal layer 233 is both electrically isolated from the overlying redistribution layer 231 and formed to be non-patterned. It is also important to note that, in order to maximize heat dissipation, this metal layer 233 is directly formed on the bottom of the dummy die to substantially cover the exposed surface located on the bottom of the dummy die. In addition, the non-patterned high thermal-conducting metal layer is formed by sputtering, a method specifically selected by Applicant to enhance heat dissipation.

The primary reference to Giri et al. discloses a multi-chip module having chips on two sides including a frame (12), a large semiconductor device (22) located above the thin-film structure, a thin-film structure (18), and a plurality of semiconductor devices (20) located below the thin-film structure. As admitted on p. 3 of the outstanding Office Action, Giri et al. does not disclose a "dummy die have a metal thermal-conducting layer directly formed thereon."

The secondary reference to Jiang et al. is cited as providing this deficiency. In response, Applicant notes that Jiang et al. teach in [0042], line 1 that the die 10 is electrically connected to the substrate 82 by the conductive trace 104. It clearly follows that the **conductive trace 104 is *electric***. As a result, the reference cannot be said to teach or suggest "the metal thermal conducting layer being electrically

isolated from the redistribution layer," as recited in claim 25. Furthermore, if Jiang were combined with Giri et al., Applicant submits that the conductive trace 104 **must be *patterned*** to form a circuit to electrically connect the semiconductor devices 20 of Giri et al. In comparison, Applicant's thermal conducting layer 233 is formed by sputtering and is a ***non-patterned layer*** because Applicant's purpose is to improve the heat dissipation (and not form electrical circuits). It follows that the reference cannot be said to teach: the metal thermal conducting layer being a non-patterned layer, as recited in claim 25.

In the outstanding Office Action, the Examiner continues to argue that the thin-film structure 18 of Giri et al. and the conductive trace 104 of Jiang et al. can be combined, by completely modifying the ***conductive*** trace 104 to be ***non-conductive*** in order to arrive at Applicant thermal conducting layer. However, the skilled artisan would clearly not be motivated to completely defeat the function of the die 10 and conductive trace 104 (i.e., to transmit an electrical signal), and use the die 10 as a non-electrical, non-patterned, thermal conducting layer. Nor has the Examiner provided any suggestion or modification, apart from Applicant's disclosure, sufficient to overcome the explicit purpose of a ***conductive*** trace 104, which teaches away from using the trace as a non-patterned, thermal conducting layer.

Jiang et al. does not teach or suggest: a flip chip package including a dummy die having an exposed surface located on a bottom thereof, the exposed surface having a metal thermal-conducting layer directly formed thereon to substantially cover the exposed surface located on the bottom of the dummy die, the metal thermal conducting layer being a non-patterned layer, the metal thermal conducting layer being electrically isolated from the redistribution layer.

Neither Klein et al., Kikuma et al., Koopmans, nor Higgins III provide the above-noted deficiencies of Giri et al. or Jiang et al.. Applicant further submits that even if the teachings of Giri et al., Jiang et al., Klein et al., Kikuma et al., Koopmans, and Higgins III were combined, as suggested by the Examiner, the resultant combination does not suggest: a flip chip package including a dummy die having an exposed surface located on a bottom thereof, the exposed surface having a metal thermal-conducting layer directly formed thereon to substantially cover the exposed

surface located on the bottom of the dummy die, the metal thermal conducting layer being a non-patterned layer, the metal thermal conducting layer being electrically isolated from the redistribution layer.

In considering the above, the Examiner is respectfully reminded that, it is a basic principle of U.S. patent law that it is improper to arbitrarily pick and choose prior art patents and combine selected portions of the selected patents on the basis of Applicant's disclosure to create a hypothetical combination which allegedly renders a claim obvious. Instead, the Supreme Court, in *KSR International Co. v. Teleflex*, 550 U.S. at ___, 82 USPQ2d at 1396, stated that:

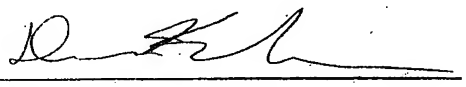
> Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis should be made explicit. See In re Kahn, 441 F. 3d 977, 988 (CA Fed. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness").

Appellant submits that the above-presented arguments clearly indicate that the Examiner has failed to provide an "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" for combining selected elements of Giri et al. with selected elements of Jiang et al, Klein et al., Kikuma et al., Koopmans, and/or Higgins III . *KSR* at 1396 (citing *In re Kahn* at 988). Clearly, such a combination is not an acceptable combination under 35 U.S.C. §103. The rejections of Appellant's claims as being rendered by the aforementioned combinations of references under 35 U.S.C. §103 are respectfully traversed.

Summary

In view of the foregoing amendments and remarks, Applicant submits that this application is now in condition for allowance and such action is respectfully requested. Should any points remain in issue, which the Examiner feels could best be resolved by either a personal or a telephone interview, it is urged that Applicant's local attorney be contacted at the exchange listed below.

Respectfully submitted,

Date: May 12, 2008 By: 

Demian K. Jackson
Reg. No. 57,551

TROXELL LAW OFFICE PLLC
5205 Leesburg Pike, Suite 1404
Falls Church, Virginia 22041
Telephone: 703 575-2711
Telefax: 703 575-2707

CUSTOMER NUMBER: 40144